07.22.05

AF 2184

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

Applicant(s): **GANTON, Robert Bruce**	Group Art Unit: **2186**
Application Serial No.: **10/085,773**	Examiner: **PATEL, Hetul B.**
Filed: **February 26, 2002**	
Title: **Memory Configuration for a Wireless Communications Device**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTION

This is an Appeal from the Examiner's Final Rejection of claims 44 - 63. The Final Rejection issued on February 17, 2005 (hereinafter "the Final Office Action"). The Notice of Appeal was received in the U.S. Patent and Trademark Office on May 20, 2005.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail (**Express Mail Label No.: EV 607321227 US**) with sufficient postage in an Express Mail envelope on **July 20, 2005** addressed to: Mail Stop Appeal Brief – Patent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Lynn Morkunas
Printed Name of Person Mailing Paper and/or Fee

Signature Lynn Morkunas

07/25/2005 EFLORES 00000137 10085773
01 FC:1402 500.00 OP

REAL PARTY IN INTEREST

The real party in interest is Kyocera Wireless Corp., a Delaware corporation, having a place of business at 10300 Campus Point Drive, San Diego, CA, 92121.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 44-63 are pending and claims 1-43 are canceled. Claims 44-63 have been finally rejected. This Appeal is directed to the rejection of claims 44-63. Claims 44-63 appear in an appendix to this Appeal Brief.

In addition, the Examiner objects to claims 49 and 50. Claims 49 and 50 contain one typographical error each in which the word "memory" is missing after "serially-addressed". These claims will have to be amended after an allowance to correct these typographical errors.

STATUS OF AMENDMENTS

Amendments to claims 44-53, 55-56, and 61 were submitted on January 14, 2005 in response to the Office Action dated September 14, 2004. The Final Office Action issued on February 17, 2005 indicated that the amendment was entered. No amendments were filed subsequent to the Final Office Action.

SUMMARY OF INVENTION

A. Brief Description

Figure 7 of Appellant's application shows a block diagram of a prior art wireless phone 10 which includes an antenna 12, a transmitter 14, a receiver 16, a microphone 18, a speaker 20, a keypad 22, a display 24, a power supply 26, and a central processing unit (CPU) 28. In addition, the cell phone 10 of the prior art includes parallel-accessible NOR-type flash memory 30. NOR-type flash memory is the dominant type of flash memory because it provides direct memory access utilizing separate parallel address, data, and control lines connection to the CPU.

In contrast, as shown in Figures 1-5, the claimed invention provides a method and system that uses serial nonvolatile memory, referred to as the serial memory 115, 215, 315, 415, 515 that is directly connected to the CPU 125, 225, 325, 425 in a portable radio telephone 100, 200, 300, 400, 500. As shown in Figure 1, a cell phone 100 includes a serial memory interface controller 105 with embedded serial memory interface logic 110. Figure 6 illustrates an example serial memory interface logic circuit 600, and the remaining communication logic of the cell phone 100 is illustrated in Figure 7. Referring again to Figure 1, the serial memory interface controller 105 is implemented as dedicated hardware so that when the cell phone 100 is powered on, the serial memory interface controller 105 loads the data stored in serial memory 115 into random access memory (RAM) 120. The stored data is utilized by the CPU (125) and other cell phone systems. Serial memory may store data representing critical operations such as an operating system or less critical data including such as phonebooks. Once the data stored in the serial memory 115 is loaded into RAM 120, the CPU 125 can execute program code and access data directly out of the RAM 120.

The serial memory may be any type of serial memory including NAND-type flash memory. NAND-type flash has relatively slow random read speeds compared to NOR-type flash memory. In addition, the interface to NAND-type flash memory is "indirect" meaning that there are no dedicated address lines or data lines as are present in a prior art NOR-type flash memory configuration. This is considered to make NAND-type flash memory relatively unsuitable for direct CPU access and execution of program code, but ideal as inexpensive storage in a mass storage system. The claimed invention overcomes the perceived deficiencies with NAND-type flash memory in wireless communication devices by directly connecting the serial memory 115 to the CPU 125.

Figures 2-4 show various embodiments of a cell phone 200 using serial memory (215, 315, 415) connected directly to the CPU (225, 325, 425). Figure 5 shows a cell phone 500 and an attachable cell phone accessory 502 that includes a serial memory 515. According to this embodiment, when the cell phone accessory 502 is attached to the cell phone 500, the contents of the serial memory 515 in the cell phone accessory 502 are loaded into onboard RAM 520 (i.e. SRAM or SDRAM), which is located in the cell phone 500. The cell phone CPU 525 can then execute program code or read data directly from the RAM 520.

Independent apparatus claims 44 and 61 set forth a communication device which utilizes a serial non-volatile memory directly connected to the processor, such that data from the serial memory is loaded into on-board random access memory upon a power up condition of the communication device. Independent method claim 56 sets forth the basic method for employing a serial non-volatile memory connected directly to a CPU.

B. Claim 44 and its dependent claims

The wireless communications device of claim 44 utilizes a serially-addressed memory directly connected to a processing unit using a serial address and data line. The processing unit has a serial memory interface for reading data from the serially-addressed memory upon a power on condition. The processing unit loads at least a portion of the data read from the serially-addressed memory into a volatile memory using parallel address and data lines connected to the processing unit. A communications circuit having a transmitter and a receiver circuit is connected to and controlled by the processing unit utilizing the at least a portion of the data read from the volatile memory.

Dependent claims 45 to 55 specify various embodiments of the communication device of independent claim 44. Specifically claims 45-50 specify the type of serially-addressed memory as one of non-volatile serial memory which may be NAND flash memory, clocked parallel memory, indexed addressable memory, and memory that is removably connected such as a multi-media card, a smart media card, a secure digital card and a memory stick. Claim 51 specifies that the volatile memory comprises at least one of a dynamic random access memory and a static random access memory. Claim 52 specifies that the power on condition triggers the processing unit to determine whether the serially-addressed memory is connected to the processing unit, and to instruct the serial memory interface to transfer the at least a portion of the data from the serially-addressed memory to the volatile memory. Claims 53-55 further define the at least a portion of the data stored in the serially-addressed memory as critical operations data or non-critical operations data.

C. Claim 56 and its dependent claims

The method for managing a wireless communications device of claim 56 executes instructions from a read-only memory in a processing unit, the instructions for directing a serial interface controller of the processing unit to read serial data from a non-volatile memory directly connected to the processing unit by a serial address and data line. The serial data is read from the non-volatile memory over the serial address and data line, is converted to parallel data, and transferred to a volatile memory over parallel address and data lines. The at least a portion of the transferred data is read from the volatile memory to operate a communications circuit of the wireless communications device in response to the at least a portion of the transferred data.

Dependent claims 57 to 60 specify various embodiments of the method of independent claim 56. Specifically claims 57 and 58 specify that the non-volatile memory is a non-volatile serial memory that may be NAND-flash memory. Claims 59 and 60 specify that the non-volatile memory is removable from the wireless communications device and may be one of a multi-media card, a smart media card, a secure digital card and a memory stick.

D. Claim 61 and its dependent claims

The wireless communications device of claim 61 comprises a wireless communications circuit which has a receiver, a transmitter, and an antenna connected to the receiver and the transmitter. The device also has a serial non-volatile memory, a volatile memory, and a processor connected to the wireless communications circuit. The processor comprises a serial interface controller directly connected to the serial non-volatile memory by a serial address and data line, and connected to the volatile memory by parallel address and data lines. The serial interface controller is configured to read serial data from the serial non-volatile memory, to convert at least a portion of the serial data to parallel data, and to store the parallel data in the

volatile memory. A read only memory stores read instructions for instructing the serial interface controller to read the serial non-volatile memory upon a boot up condition of the wireless communications device.

Dependent claims 62 and 63 specify various embodiments of the device of independent claim 61. Specifically, claims 62 and 63 specify that the serial non-volatile memory is removably connected to the serial interface controller and may be NAN flash memory.

ISSUES

(1) Whether the Examiner's rejection that claims 44-48, 50-58, 6-61 and 63 on Appeal are unpatentable under 35 U.S.C. §103(a) over U.S. Publication No. 2003/0050087 to **Kwon** in view of U.S. Publication No. 2002/0032843 to **Lofgren et al.** is erroneous.

(2) Whether the Examiner's rejection that dependent claims 49, 59 and 62 on Appeal are unpatentable under 35 U.S.C. §103(a) over **Lofgren** in view of European Application EP 1 189 465 to **Christensen** is erroneous.

GROUPING OF CLAIMS

Claims 44-63 stand or fall together, for reasons set forth in the Argument.

ARGUMENT

(1) The Rejection of Claims 44-48, 50-58, 60-61 and 63.

In paragraph 6 of the Final Office Action, Claims 44-48, 50-58, 60-61 and 63 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the Kwon Publication (USPN:2003/0050087) in view of the Lofgren Publication (USPN: 2002/0032843). Each

independent claim 44, 56, 61 comprises, inter alia, a serially-addressed memory connected directly to a processor by means of serial address and data line.

a. Rejection of Independent claims 44, 56, 61. On pages 3-4 of the Final Office Action the Examiner addresses independent claim 44, on pages 5-7 the Examiner addresses independent claim 56, and on pages 7-9 the Examiner addresses independent claim 61. The same line of reasoning of obviousness is used for each of the independent claims as discussed below.

Specifically, on pages 4, 6, and 9 of the Final Office Action, the Examiner concedes that Kwon "failed to teach that the non-volatile memory is a serially-address memory accessible by a serial address and data line and the processing unit has a serial memory interface"; that "Kwon does not teach that the method comprises a serial interface controller to read the serial data from the non-volatile memory over a serial address and data line"; and that "Kwon does not teach that the [device] comprises a serial interface controller, which is directly connected to the non-volatile memory, to read the serial data from the non-volatile memory over a serial address and data line during boot up condition". In fact, it should be noted that Kwon discloses a NAND-type flash memory 210 that interfaces with the MPU 220 in a parallel structure using the NAND interface circuit 215. (See Figure 2A of the Kwon publication.) Kwon is silent on any type of embodiment which would connect the NAND-flash directly to the CPU with a serial interface. In fact, the word "serial" does not occur anywhere in the Kwon specification. This fact is particularly significant since Appellants application, filed within six months of the Kwon application, can be considered concurrent with the Kwon application. Thus, any reference to a limitation as being "obvious to one of ordinary skill in the art at the time of the current invention was made" must be applied to the Kwon application as well. In other words, if a serial architecture is obvious at the time the invention was made, then Kwon would have disclosed

such an embodiment. But as stated above, the word "serial" does not appear anywhere in the Kwon specification.

Because a serial memory is not disclosed by Kwon, the Examiner then cites Lofgren for each independent claim 44, 56, 61. The Examiner states that "Lofgren teaches the further limitation of having a serial interface. Lofgren teaches that by having a serial interface, a controller can be designed to support memory devices of differing capacities without modifications to the system." (See, e.g., page 4, 6, 7 of the Final Office Action.) The Examiner then states for all three independent claims that "it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory modules. Also, it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous." Appellant hereby traverses each part of the Examiner's statement.

Regarding the second portion of the Examiner's statement that "it is well-known and notorious old in the art that by using a serial interface instead of parallel interface, less hardware (i.e. pin counts) is required. Therefore, it is being advantageous" does not support the Examiner's position of obviousness of the current claimed invention. For example, Appellant submits that, visa-versa, it is well-known and notoriously old in the art that a parallel interface instead of a serial interface can be advantageous in a design depending on the requirements of the design. Thus, Appellant traverses this portion of the Examiner's statement. The Examiner also includes

an Official Notice on this subject matter which is repeated for each of the independent claims 44, 56, 61 as follows:

> "[I]t is well-known and notorious old in the art that the use of a serially-addressed memory accessible by a serial address and data line instead of a parallel-addressed memory accessible by a parallel address and data line is advantageous. Compared to the parallel-addressed memory, the serially-addressed memory: (i) is cheaper so a large size of it can be used with a very little cost; (ii) using a less pin-count and (iii) has a straight forward and low cost structure. The Examiner herein taking Official Notice on this subject matter."

(See, e.g., the Final Office Action, pages 4, 6, 8). Appellant traverses this statement since, as stated above, the use of serial addressed memory has advantages in some designs, and the use of parallel addressed memory has advantages in some designs. However, whether one architecture is advantageous over another does not render the current claimed invention obvious and unpatentable, otherwise a new criterion of "advantageousness" would have to be added to the basic patent law to determine patentability.

Appellant further traverses the first portion of the Examiners statement that "it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the serial interface controller as taught by Lofgren in Kwon's device. In doing so, future memory devices of different capacities can be connected to the same controller without hardware changes resulting in forward and backward compatibility between different memory module". (Emphasis added.). Appellant respectfully points out, as stated above, that the Kwon application, concurrent with the current invention, does not implement the Lofgren serial interface in any embodiment of the Kwon device. In addition, the combination of Kwon and

Lofgren does not result in the current claimed invention without hardware changes as discussed below. The Examiner's Remarks to Applicant's assertions on page 13 of the Final Office Action merely repeat the basis for rejection as discussed above. Appellant therefore submits that the Examiner's statement of obviousness is not supportable and should be reversed.

Figures A and B of Appendix B illustrate the combination of Kwon and Lofgren as asserted by the Examiner, and one embodiment of Appellant's invention, respectively. That is, in Figure A, Appellant has replaced the parallel memory of Kwon (see Figure 2A of Kwon) with the mass storage 129 of Lofgren (see Figures 1B and 7A of Lofgren). Although the mass storage system 129 of Lofgren can possibly replace the NAND interface and the NAND flash of the Kwon device (experimentation would have to be conducted to determine whether this combination is operable) as shown in Figure A, this combination does not arrive at Appellant's invention as shown in Figure B. The two constructions, undeniably, are different, and it is not obvious to one skilled in the art to modify A to arrive at B without first having the advantage of impermissible hindsight to do so. The Examiner's approach is contrary to the enduring principle that the prior art must disclose or suggest the claimed invention in order to support an obviousness rejection. In **In re Gordon**, 733 F.2d 900, 902 (Fed. Cir. 1984), the Federal Circuit has set forth the obviousness determination rule (see also **In re Fitch**, 972 F.2d 1260 (Fed. Cir. 1992)):

> "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious *unless the prior art suggested the desirability of the modification*" (emphasis added).

The Federal Circuit has stated that even for a modification that can be characterized as "simple," the prior art must still suggest the desirability of such modification. In **In re Chu**, 66 F.3d 292,

298 (Fed. Cir. 1995), the Federal Circuit reaffirmed the rule annunciated in **In re Gordon** and provided the following guidance:

> In a proper obviousness determination, "whether the changes from the prior art are 'minor', ... the changes must be evaluated in terms of the whole invention, including whether the prior art provides any teaching or suggestion to one of ordinary skill in the art to make the changes that would produce the patentee's ... device." (citations omitted.) This includes what could be characterized as simple changes, as in *In re Gordon, 733 F.2d 900, 902, 221 U.S.P.Q. (BNA) 1125, 1127 (Fed. Cir. 1984)* **(Although a prior art device could have been turned upside down, that did not make the modification obvious unless the prior art fairly suggested the desirability of turning the device upside down).** (emphasis added.)

Appellant respectfully submits that

> "A person of ordinary skill in the art is also presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate, whether by patient, and often expensive, systematic research or by extraordinary insights, it makes no difference which." **Standard Oil Co. v. American Cyanamid Co.**, 774 F.2d 448, 454 (Fed. Cir. 1985).

Specifically, as shown in Figure A, the combination of Kwon and Lofgren would require extensive modifications to arrive at Appellant's invention as indicated by the "X" and "M" symbols of Figure A (M- modifications and X-deletions shown are not exhaustive). Specifically, Appellant asserts that, at the least, the MPU 220 would have to be modified, the controller module 133 of the combination deleted, the serial bus and the parallel bus modified, and the parallel connection to the controller module 133 deleted. However, modification of the circuit of Figure A of Exhibit 1 to arrive at Appellants invention of Figure B can only be accomplished using impermissible hindsight. That is, considered together, the collective teachings of Kwon and Lofgren do not and cannot result in the present claimed invention. The purported teachings

suggested by the Examiner are not based on anything that can be gleaned from the teachings of these references considered together. Rather, the teachings suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of appellant's disclosure, which is impermissible. Thus, independent claim 44 and its corresponding dependent claims 45-55, independent claim 56 and its corresponding dependent claims 57-60, and independent claim 61 and its corresponding dependent claims 62-63 of the present application are not rendered obvious by the disclosure of Kwon in view of Lofgren.

Finally, Appellant asserts for the record that, the Examiner has not presented a prior art reference that shows a serial memory connected directly to a CPU in a wireless device. Further, the Examiner has not presented Appellant with a reference with a NAND-type flash memory connected directly to a CPU, which is a subset of the broader claims of the serial memory connected directly to the CPU. In fact, the file history available on the USPTO PAIR web site shows that the Examiner attempted a search for such a reference on February 11, 2005. However, the Final Office Action relies upon the previously cited prior art. Appellant respectfully submits that the lack of such a reference further supports Appellant's assertion that the inventive claims under appeal are patentable and not obvious in view of the cited prior art.

Accordingly, Appellant respectfully submits that the rejection of independent claims 44, 56, and 61 under 35 U.S.C. §103(a) over the combined teachings of Kwon and Lofgren is improper and should be reversed.

b. Rejection of Dependent Claims 45-48, 50-55, 57-58, 60, 63.

On pages 9-11 of the Final Office Action the Examiner states that the combination of Kwon and Lofgren teach non-volatile serial memory that can be can be various types of serial memory including NAND-type flash, etc, that the volatile memory can be DRAM or SRAM, that

the stored data can be critical or non-critical to operation, and that a power on condition triggers determining whether memory is connected. However, as discussed above, the combination of Kwon and Lofgren does not teach serial memory directly connected to the processor. Further the combination does not teach NAND-type flash connected directly via a serial connection to memory. Additionally, these claims further limit patentable base claims and therefore, are patentable. Accordingly, Appellant respectfully submits that the rejection of claims 44-48, 50-58, 60-61 and 63 under 35 U.S.C. §103(a) over the combined teachings of Kwon and Lofgren is improper and should be reversed.

(2) **The Rejection of Claims 49, 59 and 62.**

Dependent claims 49, 59 and 62 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Lofgren in view of Christensen et al. (EP 1 189 465). The Examiner admits that the combination of Kwon and Lofgren fail to teach that the serially-addressed memory is removably connected to the processing unit as claimed in these claims and presents Christensen which discloses a removable memory having SIM card function. However, Christensen does not cure the basic deficiencies of the Kwon and Lufgren publications as discussed above. Accordingly, Appellant respectfully submits that the rejection of claims 49, 59, and 62 under 35 U.S.C. §103(a) over the combined teachings of Christensen and Lofgren is improper and should be reversed.

CONCLUSION

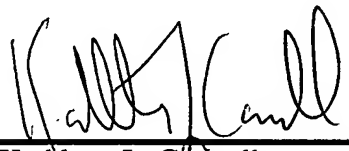
The cited references of record, considered singly or collectively, fail to disclose or in any way suggest appellant's claimed invention. Accordingly, the rejections of the appealed claims

44-63 should be reversed. Appellant respectfully requests that, with the exception of the need for correction of the two typographical errors in claims 49 and 50, claims 44-63 are allowable.

This Appeal Brief is submitted herewith in triplicate along with an Appendix A of claims on Appeal and Appendix B, and the requisite fee for filing the Appeal Brief.

Respectfully submitted,

Dated: July 20, 2005

By: 

Kathleen L. Connell
Attorney for Applicant
Reg. No.: 45,344

KYOCERA WIRELESS CORP.
Attn: Intellectual Property Department
P.O. Box 928289
San Diego, CA 92192-8289
Direct Dial: (858) 882-2169
Direct Fax: (858) 882-2485

APPENDIX A

CLAIMS ON APPEAL

44. A wireless communications device, comprising:

a serially-addressed memory for storing data, the serially-addressed memory accessible by a serial address and data line;

a processing unit directly connected to the serially-addressed memory by the serial address and data line, the processing unit having a serial memory interface for reading data from the serially-addressed memory upon a power on condition, the processing unit outputting at least a portion of the data read from the serially-addressed memory onto parallel address and data lines to a volatile memory;

the volatile memory connected to the processing unit by the parallel address and data lines, the volatile memory for storing the at least a portion of the data read from the serially-addressed memory for later use by the processing unit;

a communications circuit connected to the processing unit, the processing unit controlling the communications circuit utilizing the at least a portion of the data read from the volatile memory, the communications circuit comprising:

a transmitter circuit;

a receiver circuit; and

an antenna connected to the transmitter circuit and the receiver circuit.

45. The wireless communications device of claim 44, wherein the serially-addressed memory is non-volatile serial memory.

46. The wireless communications device of claim 45, wherein the non-volatile serial memory is serial NAND flash memory.

47. The wireless communications device of claim 44, wherein the serially-addressed memory is clocked parallel memory.

48. The wireless communications device of claim 44, wherein the serially-addressed memory is indexed addressable memory.

49. The wireless communications device of claim 44, wherein the serially-addressed is removably connected to the processing unit by the serial address and data line.

50. The wireless communications device of claim 49, wherein the serially-addressed is non-volatile serial memory comprising at least one of a multi-media card, a smart media card, a secure digital card and a memory stick.

51. The wireless communications device of claim 44, wherein the volatile memory comprises at least one of a dynamic random access memory and a static random access memory.

52. The wireless communications device of claim 44, wherein the power on condition triggers the processing unit to determine whether the serially-addressed memory is connected to the

processing unit, and to instruct the serial memory interface to transfer the at least a portion of the data from the serially-addressed memory to the volatile memory.

53. The wireless communications device of claim 44, wherein the at least a portion of the data stored in the serially-addressed memory is critical operations data.

54. The wireless communications device of claim 53, wherein the critical operations data is an application program that is critical to an operation of the wireless communications device.

55. The wireless communications device of claim 44, wherein the at least a portion of the data stored in the serially-addressed memory is non-critical operations data comprising at least one of user interface information, a recent call list, a display setting, a roaming preference, a ringer preference, a non-critical application program, and a phone book.

56. A method for managing a wireless communications device, comprising the steps of:

executing instructions from a read-only memory in a processing unit, the instructions for directing a serial interface controller of the processing unit to read serial data from a non-volatile memory directly connected to the processing unit by a serial address and data line;

reading the serial data from the non-volatile memory over the serial address and data line;

converting the serial data to parallel data;

transferring the parallel data to a volatile memory over parallel address and data lines;

reading at least a portion of the transferred data from the volatile memory; and

operating a communications circuit of the wireless communications device in response to the at least a portion of the transferred data.

57. The method of claim 56, wherein the non-volatile memory is a non-volatile serial memory.

58. The method of claim 57, wherein the non-volatile serial memory is serial NAND flash memory.

59. The method of claim 57, wherein the non-volatile memory is removable from the wireless communications device, further comprising the step of:

connecting the removable non-volatile memory to the wireless communications device.

60. The method of claim 59, wherein the removable non-volatile memory is at least one of a multi-media card, a smart media card, a secure digital card and a memory stick.

61. A wireless communications device, comprising:

a wireless communications circuit comprising:

a receiver;

a transmitter; and

an antenna connected to the receiver and the transmitter;

a serial non-volatile memory;

a volatile memory; and

a processor connected to the wireless communications circuit, the processor comprising:

a serial interface controller directly connected to the serial non-volatile memory by a serial address and data line, and connected to the volatile memory by parallel address and data lines, the serial interface controller configured to read serial data from the serial non-volatile memory, to convert at least a portion of the serial data to parallel data, and to store the parallel data in the volatile memory; and

a read only memory for storing read instructions, the read instructions for instructing the serial interface controller to read the serial non-volatile memory upon a boot up condition of the wireless communications device;

wherein the processor controls the wireless communications circuit based upon the stored parallel data in the volatile memory.

62. The wireless communications device of claim 61, wherein the serial non-volatile memory is removably connected to the serial interface controller.

63. The wireless communications device of claim 61, wherein the serial non-volatile memory is NAND flash memory.

APPENDIX B

FIGURE A (COMBINATION OF THE CITED PRIOR ART) AND

FIGURE B (APPELLANT'S CLAIMED INVENTION)